AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A durable chip pad comprising:

a terminal metal layer disposed on a passivating layer;

a diffusion barrier layer on said terminal metal layer;

a conducting layer pad on said diffusion barrier;

a hard test barrier layer on, and enclosing, said conducting layer pad, wherein said hard test barrier layer extends along the sides of said conducting layer pad and said conducting layer pad is completely enclosed by said diffusion barrier layer and said hard test barrier layer; and

a plate passivating layer on said hard test barrier layer, wherein said durable chip pad is directly probable during test without probe damage to said durable chip pad.

2. (original) A durable chip pad as in claim 1, wherein said diffusion barrier layer includes an adhesion layer on barrier metallurgy.

3. (original) A durable chip pad as in claim 2, wherein said barrier metallurgy is selected from a group of metals and metal alloys comprising titanium (Ti), titanium nitride (TiN), titanium tungsten (TiW), chromium (Cr) and tantalum/tantalum nitride (Ta/TaN).

4. (original) A durable chip pad as in claim 3, wherein said adhesion layer is selected from a group of metals and metal alloys comprising chrome-copper (CrCu), nickel vanadium (NiV) and titanium (Ti).

5. (previously presented) A durable chip pad as in claim 1, wherein said plated hard test barrier layer comprises a nickel (Ni) layer.

6. (canceled)

7. (original) A durable chip pad as in claim 1, wherein said plate passivating layer is selected from a group of metals comprising copper (Cu), ruthenium (Ru), rhodium (Rh) and gold (Au).

8. (currently amended) An integrated circuit (IC) chip with circuits formed thereon, a plurality of chip interconnect pads formed on a surface of said IC chip, one or more of said plurality of chip interconnect pads being a durable chip pad comprising:

a terminal metal layer disposed on a chip passivating layer and connecting to underlying chip wiring through a via through said chip passivating layer;

an adhesion/barrier layer on said terminal metal layer;

a seed pad on said adhesion/barrier layer;

a hard test barrier layer plated on, and enclosing, said seed pad, wherein said hard test barrier layer extends along the sides of said seed pad and said seed pad is completely enclosed by said ~~diffusion~~ adhesion/barrier layer and said hard test barrier layer; and

a plate passivating layer on said hard test barrier layer, wherein ones of said one or more are directly probable during IC performance testing and prior to any additional far back end of the line (FBEOL) processing.

9. (previously presented) An IC as in claim 8, wherein said adhesion/barrier layer includes an adhesion layer on barrier metallurgy and said barrier metallurgy is selected from a group of metals and metal alloys comprising titanium (Ti), titanium nitride (TiN), titanium tungsten (TiW), chromium (Cr) and tantalum/tantalum nitride (Ta/TaN).

10. (original) An IC as in claim 9, wherein said adhesion layer is selected from a group of metals and metal alloys comprising chrome-copper (CrCu), nickel vanadium (NiV) and titanium (Ti).

11. (previously presented) An IC as in claim 10, wherein said seed pad comprises a copper pad.

12. (currently amended) An IC as in claim I1, wherein said hard test barrier layer comprises a 0.5 – 30μm thick nickel (Ni) layer plated to and extends along the sides said copper pad.

13. (original) An IC as in claim 12, wherein said plate passivating layer is selected from a group of metals comprising copper (Cu), ruthenium (Ru), rhodium (Rh) and gold (Au).

14. (currently amended) An IC as in claim 13, wherein said IC is one of a plurality of identical ICs on a wafer, each of said plurality of identical ICs located in a die on said wafer, FBEOL processing is solder bumping and said of plurality identical ICs further comprise solder bumps formed on probed said ones.

15 – 20 (canceled)

21. (currently amended) A durable chip pad comprising:

a terminal metal layer disposed on a passivating layer;

a diffusion barrier layer on said terminal metal layer;

a copper seed layer pad on said diffusion barrier layer;

a 0.5 – 30μm thick nickel layer plated to, and enclosing, said copper seed layer pad, wherein said nickel layer extends along the sides of said copper seed layer pad and said copper seed layer pad is completely enclosed by said diffusion barrier layer and said nickel layer; and

a plate passivating layer on said nickel layer, wherein said durable chip pad is directly probable during device performance testing, prior to any additional far back end of the line (FBEOL) processing and without probe damage to said durable chip pad.

22. (previously presented) A durable chip pad as in claim 21, wherein said diffusion barrier layer includes an adhesion layer on barrier metallurgy.

23. (previously presented) A durable chip pad as in claim 22, wherein said barrier metallurgy is selected from a group of metals and metal alloys comprising titanium (Ti), titanium nitride (TiN), titanium tungsten (TiW), chromium (Cr) and tantalum/tantalum nitride (Ta/TaN).

24. (previously presented) A durable chip pad as in claim 23, wherein said adhesion layer is selected from a group of metals and metal alloys comprising chrome-copper (CrCu), nickel vanadium (NiV) and titanium (Ti).

25. (previously presented) A durable chip pad as in claim 21, wherein said plate passivating layer is selected from a group of metals comprising copper (Cu), ruthenium (Ru), rhodium (Rh) and gold (Au).